REMARKS

The examiner objects to the drawings and the specification because of various informalities.

The application includes claims 1-42 prior to entering this amendment. In the absence of indications to the contrary, the applicants assume that the examiner did not enter the amendment filed immediately prior to this amendment on August 11, 2006.

The examiner objects to claims 1, 4, 17-18 and 39 because of various informalities. The examiner rejects claims 1-4, 15-18 and 39 under 35 U.S.C. § 102(b) as being anticipated by Akimoto (U.S. Patent 5,321,664). The examiner rejects claims 5-6 and 19-20 under 35 U.S.C. §103(a) as being unpatentable by Akimoto.

The applicant amends claims 1, 2, 4-6, 15, 17-18, and 39.

The applicant cancels claims 7-14, 21-38 and 40-42, without prejudice, consistent with the response to restriction requirement filed February 7, 2006.

The application remains with claims 1-6, 15-20 and 39 after entering this amendment.

The applicants add no new matter and request reconsideration.

Drawing Objections

The applicants amend drawing Figures 1-4 and 6-8 to obviate the examiner's objections. More specifically, the applicants add the legend —PRIOR ART— to Figures 1 and 3-4 and add —MEMORY— before CONTROLLER to Figures 1-2 and 6-8. The applicants delete reference numeral 114 from the left side of the memory module MD1 in Figure 2.

Specification Objections

The applicants amend the specification to obviate the examiner's objections and to correct typographical errors. More specifically, the applicants replace various instances of "controller 704" with —controller 504— and amend the paragraph at page 6, line 3, to replace "module 706" with —module 716—.

Claim Objections

The applicants amend claims 1, 4, 17-18 and 39 to obviate the examiner's amendment. Although the applicants disagree that the second occurrence of "to" requires changing to —on—

in claims 1 and 39 or that "perpendicularly with" requires changing to —perpendicular to— in claims 4 and 18, it nonetheless does so with the understanding that the claims' scope is unaffected.

Claim Rejections Under § 102

The examiner rejects claims 1-4, 15-18 and 39 as old over Akimoto and claims 5-6 and 19-20 as obvious over Akimoto. The applicants traverse the examiner's rejections particularly as they amend the claims.

The present application describes a memory system and an associated method that eliminates stub loads that cause signal reflection by directly mounting memory ranks to motherboards that result in eliminating the need to connect memory modules to the motherboard through sockets. If there are no memory modules, then there is no need for sockets that create transmission line discontinuities. If there are no transmission line discontinuities, then no signal reflection can exist that degrade its integrity.

Akimoto, on the other hand, describes a semiconductor integrated circuit particularly useful in improving overall ASIC access time by forming a plurality of function blocks on a single semiconductor substrate. Akimoto describes an integrated circuit formed on a single substrate, while the present application describes a memory system comprised of plural integrated circuits or chips mounted directly on a motherboard.

Each of the plural integrated circuits is commonly known to be a tiny slice or chip of material on which is imprinted a complex of electronic components and their interconnections. A motherboard, circuit board, or simply board, by contrast, is an insulated board on which the plural integrated circuits or chips are mounted.

Claim 1 recites *a first buffer chip directly mounted on a motherboard, at least one first memory chip...directly mounted on the motherboard*, and *a plurality of signal traces routed on the motherboard to the first buffer and the at least one first memory chip.* Claims 15 and 39 include similar limitations. The examiner alleges Akimoto's input buffer 1B1 discloses the recited first buffer chip. Akimoto's input buffer 1B1, however, is not a chip (i.e., a packaged integrated circuit as shown in, e.g., Figures 1-2) as recited but rather a buffer circuit etched on a substrate SUB "disposed in the center of the random access memories RAM0-RAM5," resulting in a central area of the ASIC with concentrated signal conductors that complicate the layout design. Column 1, lines 64-65 and column 2, lines 14-17.

And claim 1 recites *where the system eliminates signal reflection caused by signal trace discontinuities between the first buffer and the at least one first memory device by directly mounting the first buffer and the at least one first memory device on the motherboard without an intervening socket.* Claims 15 and 39 include similar limitations. The distinction between the presently recited invention and Akimoto should be clear. While Akimoto attempts to improve the high speed operation of an ASIC by specifically arranging certain blocks on a single substrate, the present invention eliminates signal reflection caused by signal trace or transmission line discontinuities between the various chips and the motherboard by, e.g., eliminating the use of sockets between the chips and the motherboard and directly mounting the chips to the motherboard. As explained in the specification at page 4, lines 15-19, the recited system eliminates stub loads that cause signal reflection by eliminating memory modules (daughter boards mounted with chips distinct from the motherboard and mounted to the motherboard through sockets, where the sockets are directly mounted to the motherboard). As we mention above, if "there are no memory modules, then there is no need for sockets that create transmission line discontinuities. If there are no transmission line discontinuities, then no signal reflection can exist that degrade its integrity...."

Claim 3 recites *where the command and address buffer receives a command and address signal through a first command and address signal trace routed on the motherboard.* And claim 4 recites *where the at least one first memory device receives the command and address signals outputted from the command and address buffer through a second command and address signal trace routed on the motherboard* and *where the first command and address signal trace is arranged substantially perpendicular to the second command and address signal trace.* Claims 17 and 18 include similar limitations. The examiner alleges Akimoto's first signal traces RS and WS are perpendicular to second signal traces ws. Akimoto, however, gives no indication that its Figure 1 "diagram showing an ASIC memory device" indicates specific placement or arrangement of signal lines on the substrate SUB. Figure 1 is merely a block diagram showing interconnection and not necessarily placement or arrangement of the signal lines connecting the various functional blocks shown. The examiner's conclusion that Akimoto discloses signals RS and WS as perpendicular to the signals ws is improper as unsupported by the reference cited.

Moreover, claim 4 recites that the at least one first memory device receives the command and address signals *outputted* from the command and address buffer through a second command

and address signal trace. But Akimoto's buffer 1B1 does not output both command and address signals but rather only ws signals.

Claim 39 recites *a memory controller mounted directly on a motherboard and generating a plurality of command and address signals*. The applicants challenge the examiner's assertion that Akimoto discloses the memory controller inherently. While the applicants concede that additional circuitry is necessary to generate the signals input to the integrated circuit shown in Akimoto's Figure 1, they do not concede that such additional circuitry is mounted directly to the substrate SUB as would be required by the claim.

Claims 1-6, 15-20 and 39 are in condition for the examiner's allowance.

Conclusion

The applicants request reconsideration and allowance of all claims. The applicants encourage the examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

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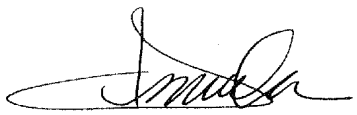

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Annotated Sheet Showing Changes

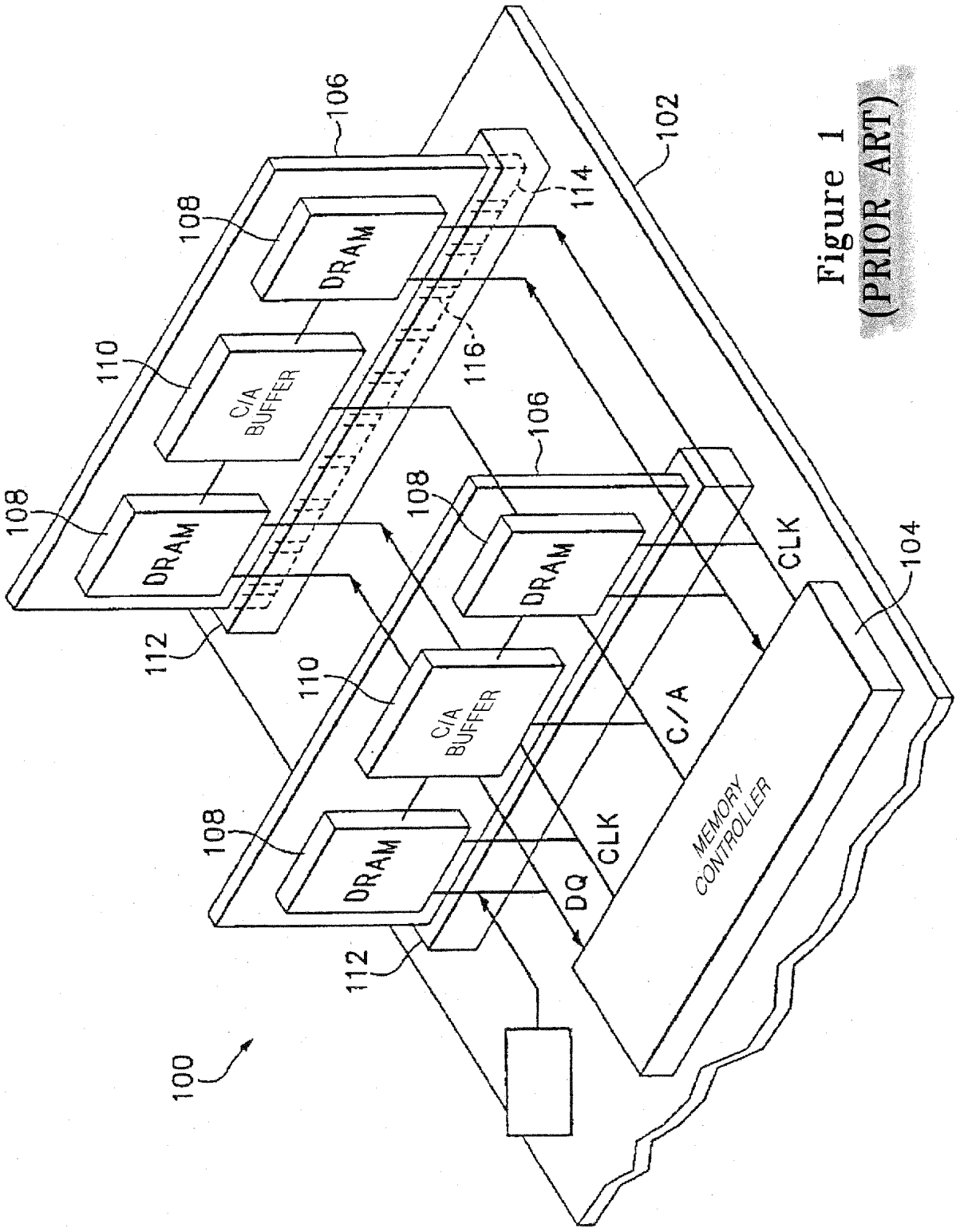

Figure 1
(PRIOR ART)

Annotated Sheet Showing Changes

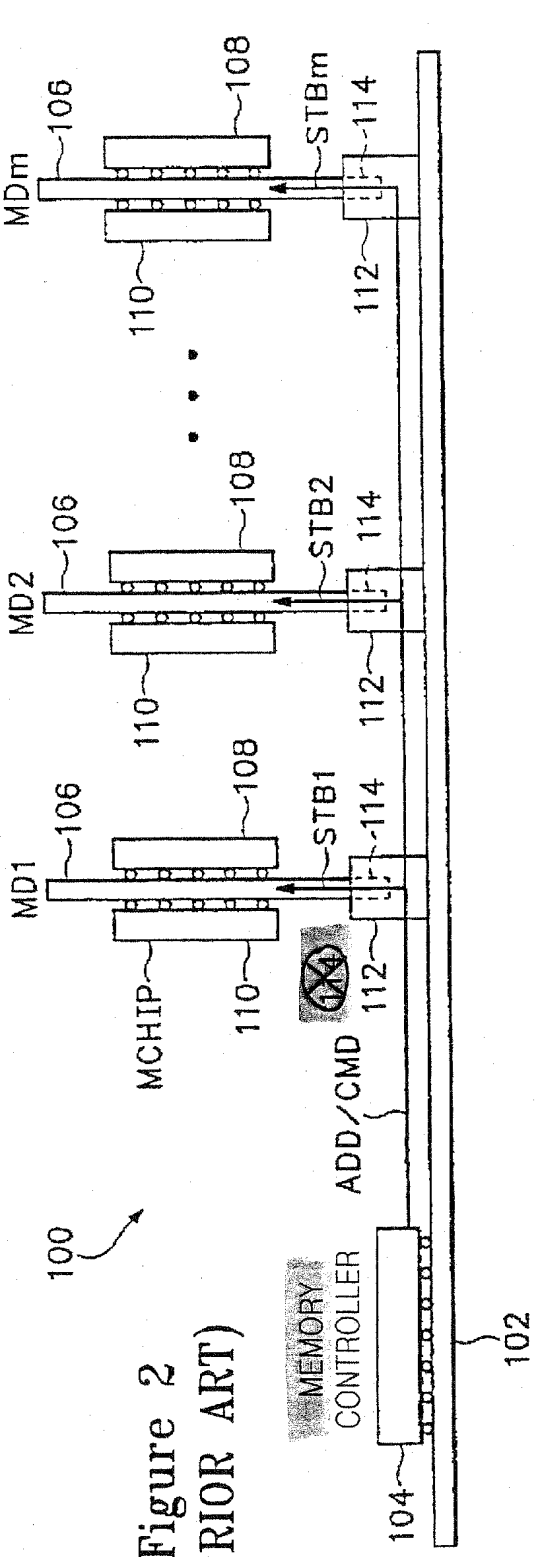

Figure 2
(PRIOR ART)

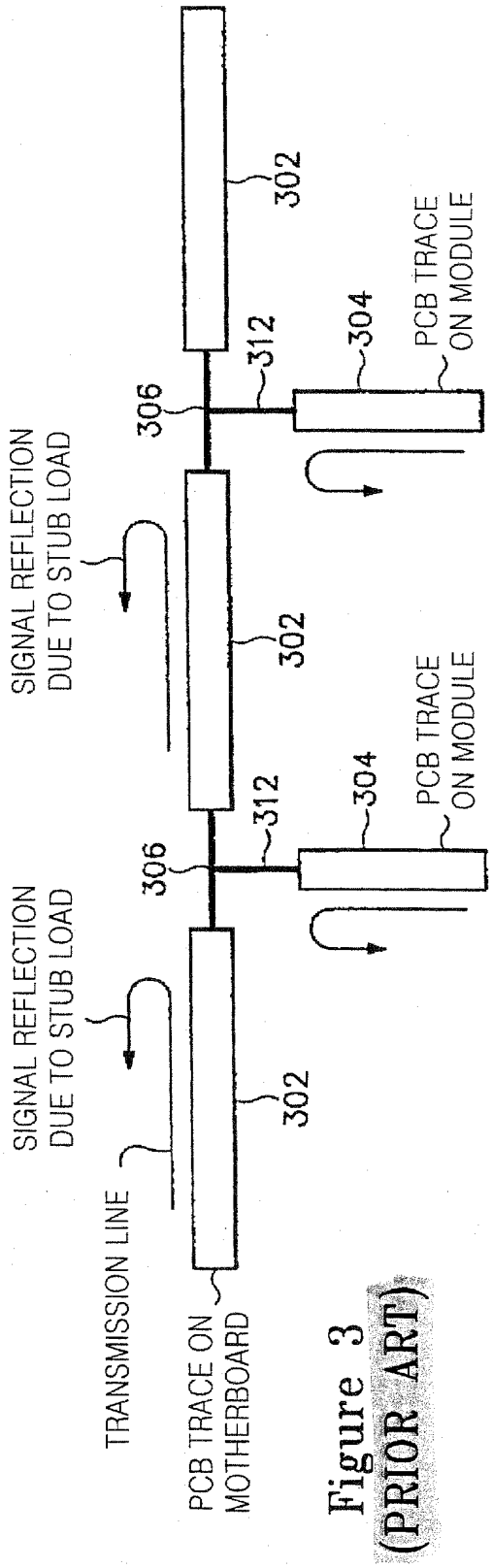

Figure 3
(PRIOR ART)

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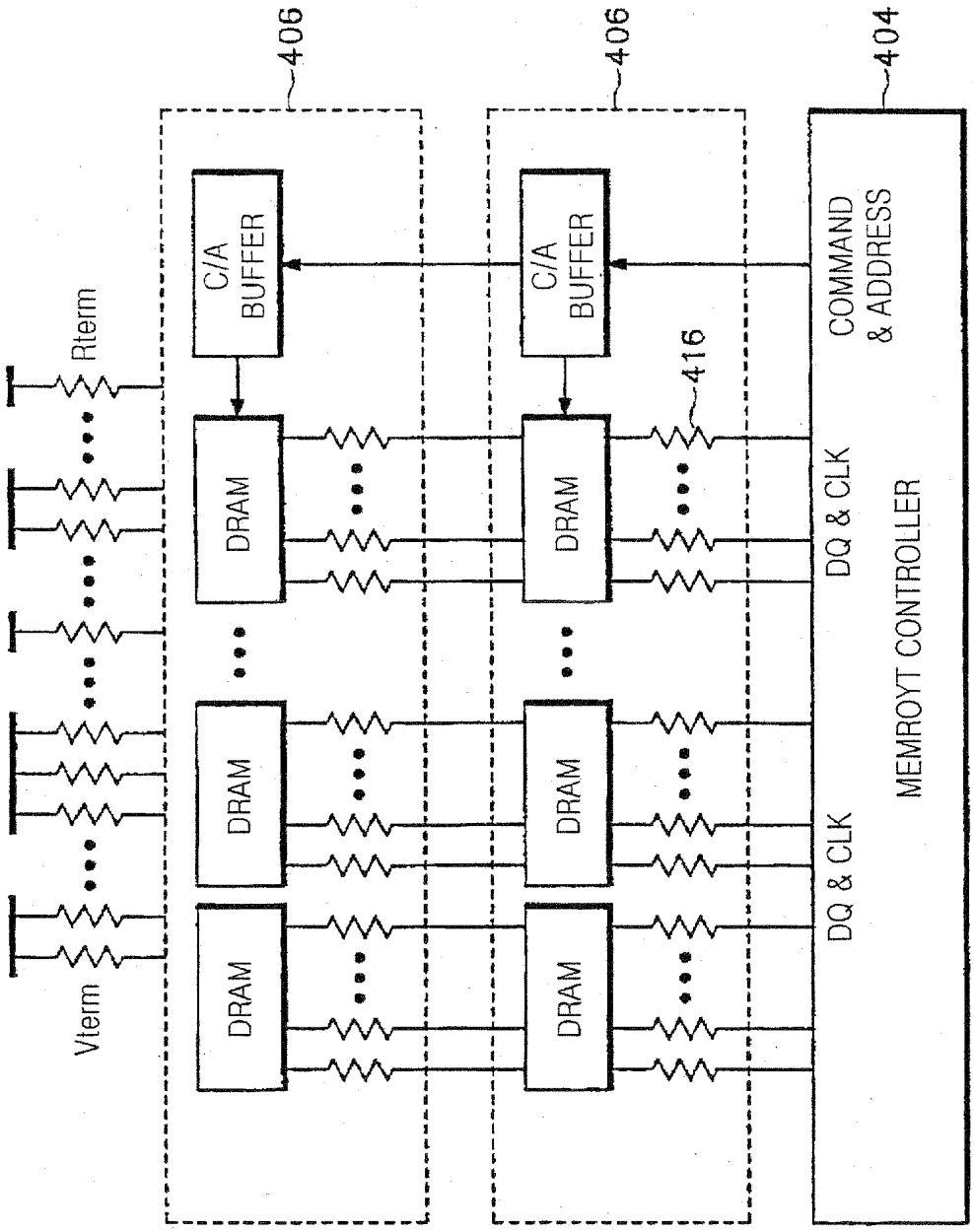

Figure 4
(PRIOR ART)

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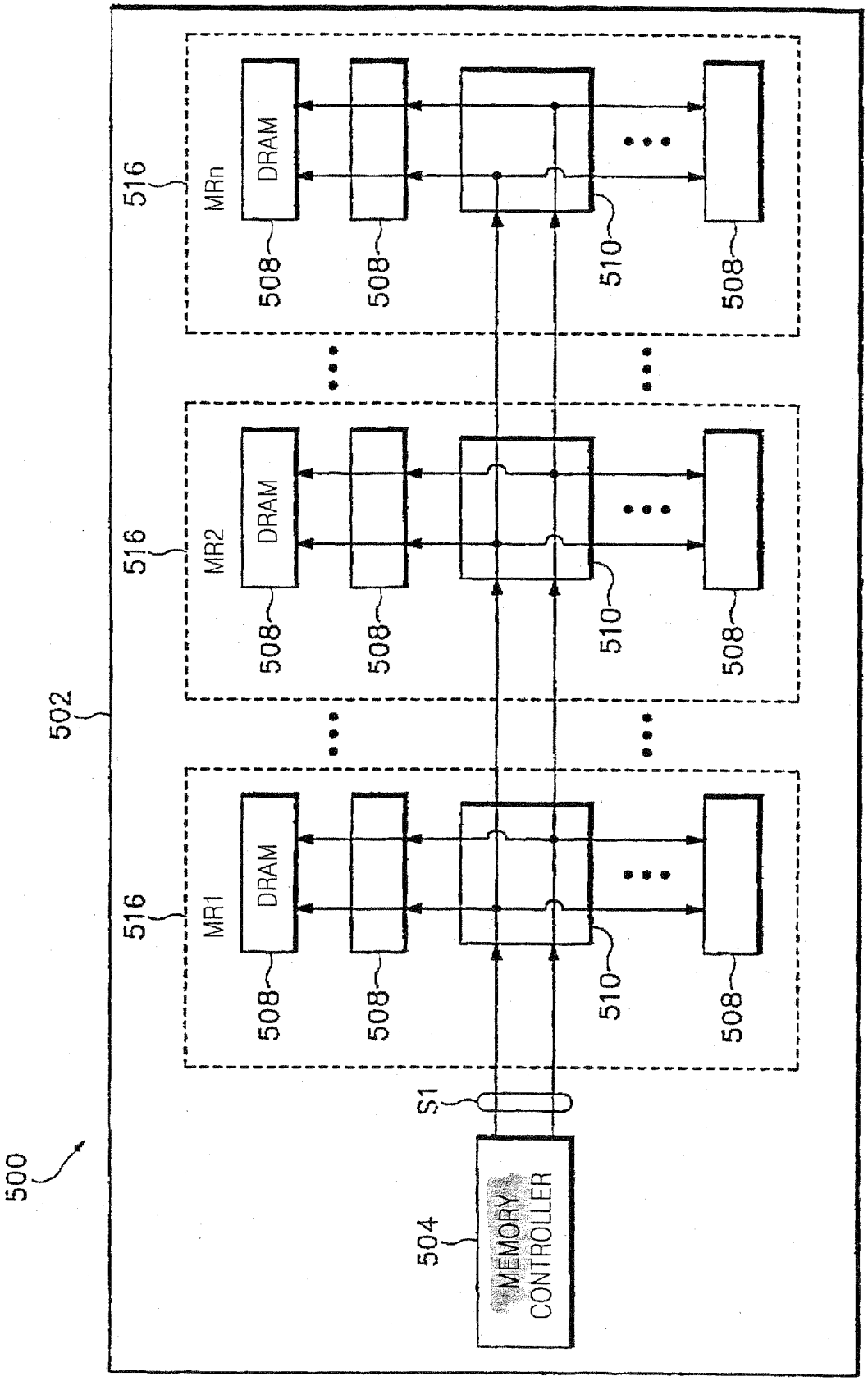

Figure 6

Annotated Sheet Showing Changes

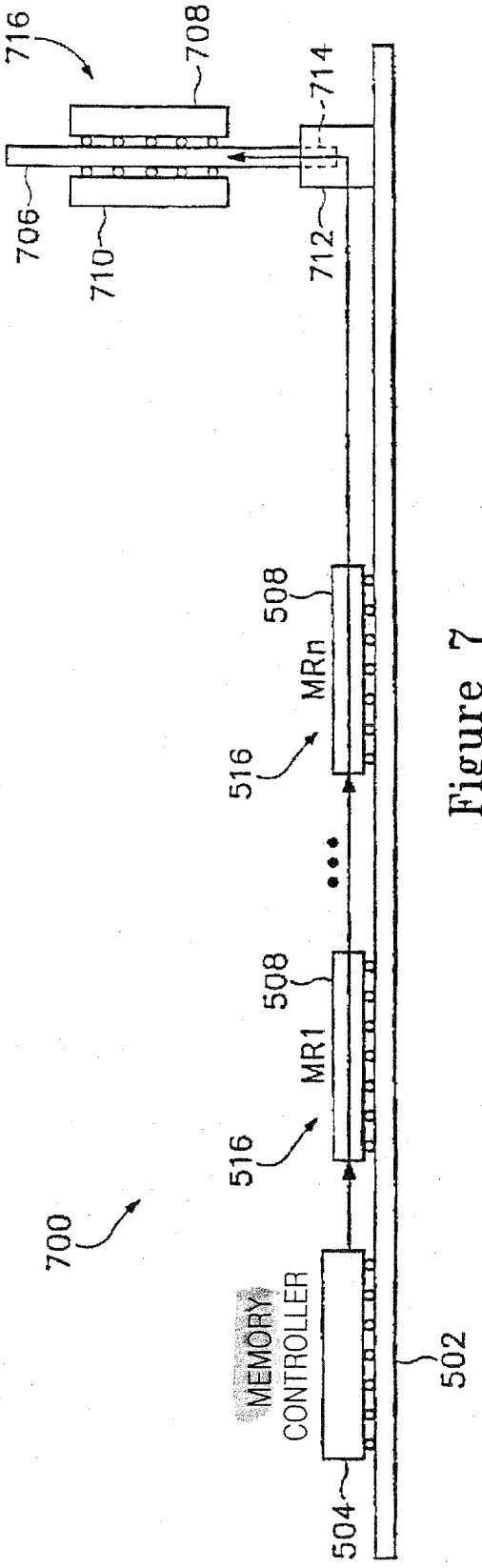

Figure 7

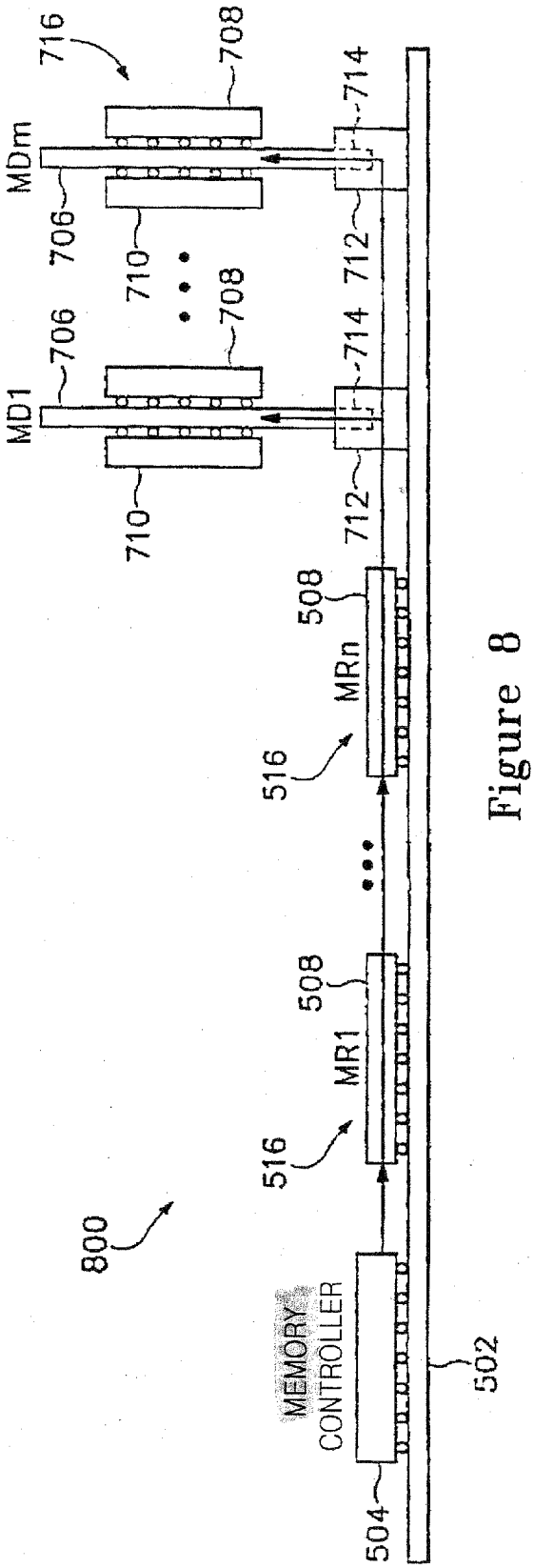

Figure 8